

XP862T Board USER'S MANUAL

V0.0d - October 14, 2005

JRM Consultants Inc.
PO Box 90310
Santa Barbara, CA 93190
(805) 564-3119 Fax (805) 962-0378
info@jrmconsultants.com
/Users/jonmiller/Desktop/manuals/xp862-v0d.txt

Table of Contents

XP862T Board

1.0 General	-
2.0 CPU Core	-
2.1 CPU	-
2.2 Primary Boot Flash Memory (512KB)	-
2.2 Secondary Ramdisk Flash Memory (8MB upto 16MB)	-
2.3 SDRAM Memory (16MB upto 64MB)	-
2.4 NVRAM Memory (8KB upto 12KB)	-
2.5 NAND Flash (8MB upto 128MB)	-
2.6 MPC860T CS Memory Map	-
2.7 MPC860T Port I/O Map	-
2.8 MPC860T Interrupts	-
3.0 Network Interfaces	-
3.1 Ethernet 100BaseT Module	-
3.2 SCC1 Ethernet 10BaseT Module	-
3.3 SMC1 Console DCE Comm Port.....	-
3.3 SMC2 Console DCE Comm Port.....	-
3.4 External Bus Master / Daughter Board Expansion Bus	-
4.0 Connectors	-

- 1) The standard board is delivered with an MPC860T 50MHz processor, 16MB of SDRAM, 8MB of Secondary Ramdisk flash and 8KB of NVRAM. The MPC862P 100MHz processor is optional.
 - 2) The standard board does NOT include the 2nd 'COM2' RS-232 port, the 10BaseT ethernet nor the NAND flash. These items are optional and loaded upon request.
 - 2) Primary Flash is pre-loaded with PPCBootn and On-Board Diagnostics.
 - 3) Secondary Flash is pre-loaded with Linux 2.4 kernel and applications.
-

2.0 CPU Core

2.1 CPU

The XP862T board is based on either the Motorola MPC860T or MPC862P processor, which combines the PowerPC core with the QUICC (Quad Integrated Communications Controller).

The XP862T board operates from a 10MHz oscillator, so the MPC860T/862P processor chip must multiply it up to the desired frequency. The MPC860T chip operates at 50MHz while the MPC862P chip may operate at 50MHz or 100MHz.

Note: Operating temperature of the MPC862P processor chip increases as the operating frequency is increased.

The RSTCONF- pin is connected to ground, to force the MPC860T to get its hard reset configuration word from the data bus. The MPC860T has internal pull-down resistors on the data bus, but some of the data lines are driven high by on-board 3 state buffers. The BPS field (D[4:5]) are configured as 8 bit boot. The DGBC bits are driven high always.

Since D[7:8] are not driven high at reset, the ISB field in the hard reset configuration word is 00, resulting in an initial IMMR value of 0x0.

Note that the MPC860T's bit numbering scheme is different than 68K-based processors. A31 and D31 are the least significant bits.

2.2 Flash Memory

The XP862T board provides 512KB of primary(boot) and 8MB of secondary flash ROM. The 512KB boot flash, Am29LV040B, resides in a 32-pin PLCC socket and is connected to CS0- with 8-bit bus width. The 8MB secondary flash is an Intel E28F64 Strataflash, it is connected to CS1 and is 16 bits wide.

2.3 SDRAM Memory

The XP862T board provides 16 Mbytes of Synchronous DRAM. The SDRAM, two Micron MT48LCM16A2TG's, is connected to CS2 and is 32 bits wide.

2.4 NVRAM Memory

The XP862T board provides a Nonvolatile Timekeeping RAM, a Dallas Semiconductor DS1743 which is

connected to a range of addresses within CS3 and is 8 bits wide.

2.5 NAND Flash

The XP860T board provides a Toshiba TC58V64 NAND Flash which is connected to a range of addresses within CS3 and is 8 bits wide.

2.6 MPC860T/862P CS Memory Map

The MPC860T/862P chip selects are organized as follows :

- 2.6.0 CS0 Boot Flash & Expansion Bus
- 2.6.1 CS1 Secondary Flash
- 2.6.2 CS2 SDRAM
- 2.6.3 CS3 NVRAM, NAND Flash, NAND Control and LEDs
- 2.6.4 CS4 n/a
- 2.6.4 CS5 Expansion Bus
- 2.6.4 CS6 Expansion Bus
- 2.6.5 CS7 Expansion Bus

2.7 MPC860T/862P Port Usage Map (Note: All signals are available at expansion connectors)

PA15	RXD1 - Enet10	PA7	
PA14	TXD1 - Enet10	PA6	RCLK1 - Enet10
PA13	RXD2 - SCC2	PA5	
PA12		PA4	TCLK1 - Enet10
PA11		PA3	
PA10		PA2	
PA9		PA1	
PA8		PA0	
PB31		PB22	
PB30		PB21	TXD2 - SMC2
PB29		PB20	RXD2 - SMC2
PB28		PB19	TENA - Enet10
PB27	FDE - Enet10	PB18	
PB26	LI - Enet10	PB17	
PB25	TXD1 - SMC1	PB16	
PB24	RXD1 - SMC1	PB15	
PB23		PB14	
PC15		PC9	
PC14		PC8	
PC13		PC7	
PC12		PC6	
PC11	COL - Enet10	PC5	
PC10	CD - Enet10	PC4	

PD15	MII_RXD[3]	PD8	MII_RX_CLK
PD14	MII_RXD[2]	PD7	MII_RX_ER
PD13	MII_RXD[1]	PD6	MII_RX_DV
PD12	MII_MDC	PD5	MII_TXD[3]
PD11	MII_TX_ER	PD4	MII_TXD[2]
PD10	MII_RXD[0]	PD3	MII_TXD[1]
PD9	MII_TXD[0]		

2.8 MPC860T/862P Interrupts

IRQ0	MII_RXD[3]
IRQ1	MII_RXD[2]
IRQ2	MII_RXD[1]
IRQ3	MII_RXD[3]
IRQ4	MII_RXD[2]
IRQ5	MII_RXD[1]
IRQ6	MII_RXD[3]
IRQ7	MII_RXD[2]

3.0 Network Interfaces

3.1 Ethernet 100BaseT Module

The Ethernet 100BaseT transceiver is implemented with the Level One LXT972 transceiver. The 100BaseT is designed to only work if an MPC860T/862P is installed as the resident processor on the board. The LXT972 interfaces to the MPC860T via its Media Independent Interface (MII). The MII is a standard interface that has been defined by IEEE specifically for this purpose. The MPC860T's MII signals are implemented via the Port D [15:3] pins, the IRQ7 pin and four other pins that are defined as 'spare' on the generic MPC860.

3.2 SCC1 Ethernet 10BaseT Module

The Ethernet 10BaseT transceiver is implemented with the Level One LXT905 transceiver. The Ethernet 10BaseT transceiver uses nine I/O signals from the MPC860T for data transmission and configuration. The following pins are used:

PA15	RXD1
PA14	TXD1
PA6	CLK2 (Receive Clock)
PA4	CLK4 (Transmit Clock)
PB19	RTS1 (TENA)
PC11	CTS1 (CLSN)
PC10	CD1 (RENA)
PB27	FDE- (set output low for full duplex)
PB26	Link Test Enable (normally high output)

3.3 SMC1 Console DCE Comm Port

A serial link to a Console Device is enabled by attaching the transmit and receive signals to a DCE connector.

PB25	SMTXD1
PB24	SMRXD1

3.4 SMC2 Console DCE Comm Port

A serial link to a Console Device is enabled by attaching the transmit and receive signals to a DCE connector.

PB21	SMTXD2
PB20	SMRXD2

3.5 Daughter Board / External Bus Master Expansion Bus

An Expansion Port is provided to allow attachment of a variety of daughter board types and for External Bus Masters such as the PLX-9054, PCI Bridge controller. The expansion port allows for an external TDM highway, serial connections and also general purpose parallel port connections via a high density 60 pin socket. The part number for the mating header required on any daughter board is SAMTEK TFM-130-32-S-D-LC.

All necessary 860 signals are brought to enable any type of expansion device including external bus masters such as a PCI Bridge, or video DSP, or PCMCIA or others.

Also power(5V & 3.3V) and ground are available to facilitate implementation of daughterboards.

=====

4.0 Connectors

4.1 Background Debug Mode (BDM) Connector, J1

A 10-pin BDM Connector, J1, is provided with the Motorola-defined pinout :

1	VFLS0	2	SRST-
3	GND	4	DSCK-
5	GND	6	VFLS1
7	HRST-	8	DSDI
9	VDDH	10	DSDO

4.2 10BaseT Ethernet Connector, J8

J5 is an RJ45 modular jack, with the standard 10BaseT pin assignments:

1 - TX+	5 - NC
2 - TX-	6 - RX-
3 - RX+	7 - NC
4 - NC	8 - NC

4.3 10BaseT Ethernet Connector, J4

J4 is an RJ45 modular jack, with the standard 10BaseT pin assignments:

1 - TX+	5 - NC
2 - TX-	6 - RX-
3 - RX+	7 - NC
4 - NC	8 - NC

4.4 SMC1 Comm Port Connector, J5

SMC1 is connected to a 9-position DB9 female connector, J4, through an RS-232 transceiver. The pin assignments of the connector are:

1 - NC	6 - NC
2 - PB25 (SMTXD1)	7 - NC
3 - PB24 (SMRXD1)	8 - NC
4 - NC	9 - NC
5 - Gnd	

4.5 SMC2 Comm Port Connector, J6

SMC1 is connected to a 9-position DB9 female connector, J4, through an RS-232 transceiver. The pin assignments of the connector are:

1 - NC	6 - NC
2 - PB25 (SMTXD1)	7 - NC
3 - PB24 (SMRXD1)	8 - NC
4 - NC	9 - NC
5 - Gnd	

4.6 Expansion Bus Connectors, JSA & JSB (Daughter Boards / External Bus Masters)

(100 pin SamTec SFM-150-L2-S-D-LC sockets)

JSA Conn				JSB Conn			
ground	1	2	ground	ground	1	2	ground
ground	3	4	ground	ground	3	4	ground
A31	5	6	A30	PA15	5	6	PA14
A29	7	8	A28	PA13	7	8	PA12
A27	9	10	A26	PA11	9	10	PA10
A25	11	12	A24	PA9	11	12	PA8
A23	13	14	A22	PA7	13	14	PA6
A21	15	16	A20	PA5	15	16	PA4
A19	17	18	A18	PA3	17	18	PA2
A17	19	20	A16	PA1	19	20	PA0
A15	21	22	A14	PB31	21	22	PB30
A13	23	24	A12	PB29	23	24	PB28
TSIZ0	25	26	TSIZ1	PB27	25	26	PB26
BDIP	27	28	TS-	PB25	27	28	PB24
RW-	29	30	BURST	PB23	29	30	PB22
TA-	31	32	TEA-	PB21	31	32	PB20
BI-	33	34	BB-	PB19	33	34	PB18
BR-	35	36	BG-	PB17	35	36	PB16
AS-	37	38	IRQ2-	PB15	37	38	PB14
IRQ4-	39	40	IRQ6-	WAIT_A-	39	40	WAIT_B-
CS0-	41	42	CS5-	MODCK1	41	42	MODCK2
CS6-	43	44	CS7-	OP0	43	44	OP1
HRESET-	45	46	XXP2-	CE1_A-	45	46	GPL_A4-
XCLK	47	48	XXP3-	CE2_A-	47	48	GPL_A5-

+3.3V	49 50	+3.3V	+5V	49 50	+5V
+3.3V	51 52	+3.3V	+5V	51 52	+5V
BS_B0-	53 54	BS_B1-	IP_A0	53 54	IP_A1
BS_B2-	55 56	BS_B3-	IP_A2	55 56	IP_A3
GPL_A0-	57 58	GPL_A1-	IP_A4	57 58	IP_A5
GPL_A2-	59 60	GPL_A3-	IP_A6	59 60	IP_A7
DP1	61 62	DP0	IP_B0	61 62	IP_B1
DP3	63 64	DP2	IP_B2	63 64	IP_B3
D1	65 66	D0	IP_B4	65 66	IP_B5
D3	67 68	D2	IP_B6	67 68	IP_B7
D5	69 70	D4	ALE_A	69 70	ALE_B
D7	71 72	D6	PC4	71 72	PC5
D9	73 74	D8	PC6	73 74	PC7
D11	75 76	D10	PC8	75 76	PC9
D13	77 78	D12	PC10	77 78	PC11
D15	79 80	D14	PC12	79 80	PC13
D17	81 82	D16	PC14	81 82	PC15
D19	83 84	D18	XXP1-	83 84	GPL_B4-
D21	85 86	D20	A1	85 86	A0
D23	87 88	D22	A3	87 88	A2
D25	89 90	D24	A5	89 90	A4
D27	91 92	D26	A7	91 92	A6
D29	93 94	D28	A9	93 94	A8
D31	95 96	D30	A11	95 96	A10
ground	97 98	ground	ground	97 98	ground
ground	99 100	ground	ground	99 100	ground

JSA Conn

JSB Conn

(100 pin SamTec SFM-150-L2-S-D-LC sockets)

Note that the MPC860T's bit numbering scheme is different than 68K-based processors. A31 and D31 are the least significant bits!!

4.7 Power Connections

The XP860T Board operates from +5 volts regulated DC which may be provided from a wall transformer power supply via the 2.0 mm jack, J3, or from a standard PC power supply via the 4 pin Molex connector, J2.

4.7.1 Power Jack, J3

A 2.0 mm jack (J3) is provided for powering the board through an external +5VDC regulated power supply.

4.7.2 Molex Power Connector, J2

A 4 pin Molex connector (J2) allows 5 volts to be obtained from the Disc Drive power connector of a standard PC power supply.

=====

5.0 Mechanical

The XP860T Board is packaged in the same footprint as a 6U Compact PCI board (6.3" by 9.1") but without the backplane connector. The Compact PCI form factor allows use of off-the-shelf cabinets for the racking of multiple cards. I/O and power connections are along the back edge. LED displays, the operator console connector and the multi-protocol communications connector are along the front edge.

6.0 PPCBoot Boot Flash Resident

PPCBoot 1.1.4 (May 13 2004 - 17:27:09)

XP860T Port, Copyright 2002 Simple Network Magic Corporation

CPU: unknown MPC860 (0x07000003) at 50 MHz: 16 kB I-Cache 8 kB D-Cache FEC present

*** Warning: CPU Core has Silicon Bugs -- Check the Errata ***

Board: ### No HW ID - assuming XP860T

DRAM: 16 MB

Top of RAM usable for PPCBoot at: 01000000

Reserving 256k for PPCBoot at: 00fc0000

Reserving 132k for malloc() at: 00f9f000

Reserving 64 Bytes for Board Info at: 00f9efc0

Stack Pointer at: 00f9efa8

New Stack Pointer is: 00f9efa8

Now running in RAM - PPCBoot at: 00fc0000

FLASH: 8 MB

In: serial

Out: serial

Err: serial

PPCBoot relocated to 00fc0000

7.0 Diagnostics Boot Flash resident

Type "run diags" to run in diagnostics mode

Hit any key to stop autoboot: 5 4 3 2 1 0

Booting image at fff30000 ...

Image Name: diags

Created: 2005-02-11 0:52:27 UTC

Image Type: PowerPC PPCBoot Standalone Program (gzip compressed)

Data Size: 64228 Bytes = 62 kB = 0 MB

Load Address: 00002000

Entry Point: 00002000

Verifying Checksum ... OK

Uncompressing Standalone Application ... OK

Calculated CPU speed: 50000000

Synchronizing PPC RTC to external RTC..
Checking for daughterboard..
Red Box daughterboard detected.
MPC860 power-up diagnostics: Version 1.1.1 (c) 2002 - 2004 VCT Labs, Inc.
Memory : Quick Test: PASSED
Memory : DMA: PASSED
FEC Ethernet : Exerciser Test: PASSED

Control returned to monitor...
Booting image at d0000000 ...

8.0 Linux 2.4 RamDisk Flash resident

Image Name: redbox kernel with scc2 console
Created: 2004-01-22 7:24:37 UTC
Image Type: PowerPC Linux Kernel Image (gzip compressed)
Data Size: 487417 Bytes = 475 kB = 0 MB
Load Address: 00000000
Entry Point: 00000000
Verifying Checksum ... OK
Uncompressing Kernel Image ... OK
Current stack ends at 0x00F9ED98 => set upper limit to 0x00800000
cmdline at 0x007FFF00 ... 0x007FFF0D
Loading RAMDisk Image at d00a0000 ...
Image Name: Tiny filesystem for working on P
Created: 2003-11-12 23:08:47 UTC
Image Type: PowerPC Linux RAMDisk Image (gzip compressed)
Data Size: 152382 Bytes = 148 kB = 0 MB
Load Address: 00000000
Entry Point: 00000000
Verifying Checksum ... OK
initrd at 0xD00A0040 ... 0xD00C537D (len=152382=0x2533E)
Loading Ramdisk to 00f79000, end 00f9e33e ... OK
bd address = 0x007FFEC0
memstart = 0x00000000
memsize = 0x01000000
flashstart = 0xFFFF0000
flashsize = 0x00800000
flashoffset = 0x00040000
sramstart = 0x00000000
sramsize = 0x00000000
immr_base = 0xF0000000
bootflags = 0x00000001
intfreq = 50 MHz
busfreq = 50 MHz
ethaddr = 00:11:22:33:44:55
IP addr = 192.168.1.22
baudrate = 57600 bps
getc = 0x00FD6680
tstc = 0x00FD66C4
putc = 0x00FD65E8

```
puts      = 0x00FD66EC
printf    = 0x00FCE8BC
install_hdlr= 0x00FD61D8
free_hdlr  = 0x00FD6264
malloc    = 0x00FC2690
free      = 0x00FC2B70
## Transferring control to Linux (at address 00000000) ...
init started: BusyBox v1.00-pre3 (2003.11.12-18:53+0000) multi-c
linuxrc: Bummer, can't write to log on /dev/tty5!
```

Please press Enter to activate this console.
Starting pid 11, console /dev/console: '/bin/sh'

Process '/bin/sh' (pid 11) exited. Scheduling it for restart.

Please press Enter to activate this console.
linuxrc: Bummer, can't write to log on /dev/tty5!

BusyBox v1.00-pre3 (2003.11.12-18:53+0000) Built-in shell (ash)
Enter 'help' for a list of built-in commands.

```
# ls -l
drwxrwxr-x  2 0      0      1024 var
drwxrwxr-x  2 0      0      1024 usr
drwxrwxr-x  2 0      0      1024 tmp
dr-xr-xr-x 21 0      0          0 proc
drwxrwxr-x  2 0      0      1024 etc
drwxrwxr-x  2 0      0      1024 dev
drwxrwxr-x  2 0      0      1024 bin
lrwxrwxrwx  1 0      0          12 linuxrc -> /bin/busybox
```

#
